[Attorneys Listed On Signature Page]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

RAMBUS INC.,

Plaintiff,

v.

HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR MANUFACTURING AMERICA INC.,

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, L.P.,

NANYA TECHNOLOGY CORPORATION, NANYA TECHNOLOGY CORPORATION U.S.A.,

Defendants.

Case No. C 05-00334 RMW

JOINT MOTION OF HYNIX, MICRON, AND SAMSUNG FOR SUMMARY JUDGMENT OF INVALIDITY UNDER 35 U.S.C. § 102 OF CLAIM 14 OF THE '184 PATENT, CLAIM 33 OF THE '120 PATENT, CLAIM 16 OF THE '863 PATENT, CLAIM 3 OF THE '446 PATENT, CLAIM 43 OF THE '051 PATENT, AND CLAIM 34 OF THE '037 PATENT (MSJ #2)

Hearing Date: December 2, 2008
Time: 9:00 a.m.
Courtroom: 6
Judge: Hon. Ronald M. Whyte

RAMBUS INC., Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, L.P., Defendants.	Case No. C 05-02298 RMW
RAMBUS INC., Plaintiff, v. MICRON TECHNOLOGY, INC. and MICRON SEMICONDUCTOR PRODUCTS, INC., Defendants.	Case No. C 06-00244 RMW

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TABLE OF AUTHORITIES

TO RAMBUS, INC. AND ITS ATTORNEYS OF RECORD:

NOTICE OF MOTION

NOTICE IS GIVEN THAT defendants Hynix Semiconductor Inc., Hynix Semiconductor America Inc., Hynix Semiconductor Manufacturing America Inc. (collectively "Hynix"), Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, L.P. (collectively "Samsung"), Micron Technology, Inc. and Micron Semiconductor Products, Inc. (collectively "Micron") (hereby move the Court for summary judgment of invalidity of certain asserted claims of U.S. Patent Nos. 6,182,184 ("the '184 patent"), 6,324,120 ("the '120 patent"), 6,452,863 ("the '863 patent"), 6,546,446 ("the '446 patent"), 6,584,037 ("the '037 patent") and 6,314,051 ("the '051 patent"), pursuant to Federal Rule of Civil Procedure 56. Specifically, Hynix, Micron, and Samsung seek a judgment that claim 14 of the '184 patent, claim 33 of '120 patent, claim 16 of the '863 patent, claim 3 of the '446 patent, claim 43 of the '051 patent, and claim 34 of '037 patent (collectively "asserted claims at issue") are anticipated by U.S. Patent No. 4,663,735 to Novak et al. and are therefore invalid under 35 U.S.C. § 102. This motion shall be heard on December 2, 2008, in the above-referenced court, located at 280 South First Street, San Jose, California 95110.

Hynix, Micron, and Samsung base their motion on this Notice of Motion and Motion, the Memorandum of Points and Authorities, the accompanying Declaration of Theodore G. Brown III in Support of Motion for Summary Judgment on Invalidity and *Daubert* Motions ("Brown Decl.") and Declaration of Joseph McAlexander in Support of Joint Motion of Hynix, Micron, and Samsung for Summary Judgment of Invalidity Under 35 U.S.C. § 102 of Claim 14 of the '184 Patent, Claim 33 of the '120 Patent, Claim 16 of the '863 Patent, Claim 3 of the '446 Patent, Claim 43 of the '051 Patent, and Claim 34 of the '037 Patent (MSJ #2) ("McAlexander Decl."), and on such other evidence and argument that may properly come before the Court.

MEMORANDUM OF POINTS AND AUTHORITIES

I. STATEMENT OF ISSUES TO BE DECIDED

Whether the asserted claims at issue are anticipated by U.S. Patent No. 4,663,735 ("Novak") under 35 U.S.C. § 102.

II. INTRODUCTION AND SUMMARY OF ARGUMENT

Defendants Hynix, Micron, and Samsung move for summary judgment that the asserted claims are invalid as anticipated by Novak.

As shown more fully below, each and every limitation of the asserted claims are present in the Novak patent. In fact, this Court has already determined that many of the limitations of the asserted claims were disclosed in U.S. Patent No. 4,330,852 ("Redwine"), which shares many of the same features disclosed in Novak. There is no genuine issue of material fact regarding the disclosure of the relevant limitations in Novak. Accordingly, this joint motion for summary judgment should be granted, and the aforementioned asserted claims should be declared invalid.

III. STATEMENT OF RELEVANT FACTS

The Novak patent, U.S. Patent No. 4,663,735, was filed December 30, 1983 and issued May 5, 1987, well over one year before the filing of the initial Rambus patent application in April, 1990. (Brown Decl. Ex. T, Novak.) As such, Novak is prior art to the asserted Rambus patents under 35 U.S.C. § 102(b). Novak discloses a synchronous DRAM (dynamic random access memory) chip that can be used as a VRAM (video random access memory). The DRAM chip receives block size information and employs dual edge clocking. (McAlexander Decl. Ex. 1, Corrected Expert Report of Joseph McAlexander Regarding Invalidity of U.S. Patent Numbers 6,038,195; 6,182,184; 6,266,285; 6,314,051; 3,324,120; 6,378,020; 6,426,916; 6,452,863; 6,546,446; 6,584,037; 6,697,295; 6,715,020; 7,751,696; 6,493,789; 6,496,897 (hereinafter "McAlexander Report") ¶ 296.) Novak also discloses the precharging functions recited in the asserted claims as well as the predetermined delay of write operations. (*Id.*)

The Redwine patent, U.S. Patent No. 4,330,852, was filed on November 23, 1979 and issued on May 18, 1982. (Brown Decl. Ex. V, Redwine; McAlexander Decl. ¶ 3.) Redwine, similar to Novak, was filed before the filing of the initial Rambus patent application. The Novak and Redwine

references, which were both assigned to Texas Instruments and relate to DRAM chips used as VRAMs, are similar in many respects. In particular, Figure 2 of Novak is virtually identical to Figure 1 of Redwine. (Brown Decl. Ex. T, Novak Fig 2; Brown Decl. Ex. V, Redwine Fig. 1.) Additionally, Figure 4 in Novak has many of the same timing diagrams as Figure 2 in Redwine. (McAlexander Decl. ¶ 3; Brown Decl. Ex. T, Novak Fig. 4; Brown Decl. Ex. V, Redwine Fig. 2.) In fact, on February 28, 2006, this Court determined that Redwine disclosed an external clock signal and operation code, which are two elements that are disclosed in Novak, and which are also present in the claims at issue. (Brown Decl. Ex. S, Court's February 28, 2006 Order Denying Hynix's Motion for Summary Judgment of Invalidity of U.S. Patent Nos. 6,378,020 and 5,915,105 Under 35 U.S.C. §§102 and/or 103 in Case No. C 00-20905 RMW (hereinafter "Redwine MSJ Order.")).

IV. SUMMARY OF RELEVANT LAW

A. Validity Under 35 U.S.C. § 102

Anticipation under 35 U.S.C. § 102 requires that each and every element of the claimed invention must be disclosed in a single prior art reference. *Minnesota Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992). The claimed elements must be either inherent or disclosed expressly in the prior art reference. *Id.*; *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Cir. 1988); *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995) ("[a] reference anticipates a claim if it discloses the claimed invention 'such that a skilled artisan could take its teachings in *combination with his own knowledge of the particular art and be in possession of the invention*'") (quoting *In re LeGrice*, 301 F.2d 929, 936 (C.C.P.A. 1962) (emphasis in original)); *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339 (Fed. Cir. 2000) (A publication that does not expressly disclose in words one or more elements of a patent's claims may nonetheless anticipate if a person of ordinary skill in the art would understand the publication to disclose the missing element and if such a person could have combined the publication's description with his own knowledge to make the invention). However, the test for anticipation does not require that the prior art reference duplicate word for word what is in the claims. *Akzo N.V. v. United States Int'l Trade Comm'n*, 808 F.2d 1471, 1479 & n.11 (Fed. Cir. 1986).

It is the ***claims*** of the patent that define the invention, and it is the ***claims***, not the specification,

which must be anticipated. *Constant*, 848 F.2d at 1570-71. A claim may not be redrafted, by the patentee or the judge, for purposes of avoiding an anticipatory prior art reference and it is improper to incorporate limitations from the specification into the issued claims in order to avoid a finding of anticipation. *Id.*; *Quantum Corp. v. Rodime PLC*, 65 F.3d 1577, 1584 (Fed. Cir. 1995). The patent owner cannot rehabilitate the claim by pointing to unclaimed features shown or described elsewhere in the patent specification to give narrower meaning to the claim language. *Constant*, 848 F.2d at 1570-71.

B. Summary Judgment

Under Fed. R. Civ. P. 56, where there is no genuine dispute as to any material fact concerning an issue, the moving party is entitled to summary judgment on that issue. Fed. R. Civ. P. 56(c); *Celotex Corp. v. Catrett*, 477 U.S. 317, 322 (1996); *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 247-248 (1986); *Matsushita Electric Industries v. Zenith Radio Corp.*, 475 U.S. 574, 585-87 (1996); *Ragas v. Tenn. Gas Pipeline Co.*, 136 F.3d 455, 458 (5th Cir. 1998). Rule 56 mandates the entry of summary judgment against a party "who fails to make a showing sufficient to establish the existence of an element essential to that party's case, and in which that party will bear the burden of proof at trial." *Id.*

Initially, the moving party must state the basis of the motion and demonstrate the absence of a genuine issue. *Celotex*, 477 U.S. at 323. Fed. R. Civ. P. 56(e) requires the nonmoving party to go beyond the pleadings, and by affidavits, depositions, answers to interrogatories, and admissions, designate specific facts showing there is a genuine issue for trial. *Id.* at 324. The court must view all evidence in the light most favorable to the non-moving party, and all reasonable inferences must be drawn in favor of the party opposing the motion. *Matsushita*, 475 U.S. at 587-588. But a genuine issue sufficient to preclude summary judgment is not created by unsupported speculation or by improbable inferences; the evidence taken as a whole must be sufficient that a reasonable trier of fact could find for the party opposing the motion as to that particular fact. *Matsushita*, 475 U.S. at 586-587.

Summary judgment "is as appropriate in a patent case as in any other where no genuine issue of material fact is present and the movant is entitled to judgment as a matter of law." *Townsend Eng'g*

Co. v. HiTech Co., 829 F.2d 1086, 1089 (Fed. Cir. 1987); *see*, *e.g.*, *Constant,* 848 F.2d at 1560 (summary judgment of invalidity). For anticipation, ‘‘[f]or summary determination to be proper, there must be no genuine dispute whether the limitations of the claimed invention are disclosed, either explicitly or inherently, by an allegedly anticipating prior art reference.’’) *Hazani v. U.S. Int’l Trade Comm’n*, 126 F.3d 1473, 44 USPQ2d 1358 (Fed. Cir. 1997); *see also General Elec. Co. v. Nintendo Co., Ltd.*, 179 F.3d 1350, 1353 (Fed. Cir. 1999) (“Although anticipation is a question of fact, it still may be decided on summary judgment if the record reveals no genuine dispute of material fact.”).

V. ARGUMENT

A. NOVAK ANTICIPATES ASSERTED CLAIM 14 OF THE ‘184 PATENT

Independent claim 13 and dependent, asserted claim 14 of the '184 patent are invalid under 35 U.S.C. § 102 because each and every limitation of those claims is disclosed by the Novak patent. *Minnesota Mining & Mfg. Co.,* 976 F.2d at 1565. The following table provides the language of claims 13 and 14 of the '184 patent and the corresponding claim constructions:

‘184 Claim Language	Claim Constructions
13[a] A method of operation of a memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:	"memory device" means "a device in which information can be stored and retrieved electronically" “memory cells” means “electronic storage elements in a memory array”
[b] receiving first block size information from a master, wherein the first block size information defines a first amount of data to be sampled by the memory device in response to a write request	“block size information” means “information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request” “data” means “one or more bits written to/read from the memory array “sample” means “to obtain at a discrete point in time” “write request” means “a series of bits used to request a write of data to a memory device”
[c] receiving a first write request from the master; and	“write request” means “a series of bits used to request a write of data to a memory device”
[d] sampling a first portion of the first amount of data synchronously with respect to a first transition of an external clock signal and a second portion of the first amount of data synchronously with respect to a second transition of the external clock signal.	"sample" means "to obtain at a discrete point in time" "data" means "one or more bits written to/read from a memory array" "synchronously with respect to" means "having a known timing relationship with respect to" "external clock signal" means "a periodic signal from a source external to the device to provide timing information"

'184 Claim Language	Claim Constructions
14. The method of claim 13 wherein the first transition of the external clock signal is a rising edge transition and the second transition of the external clock signal is a falling edge transition.	

1. Novak Discloses the Limitations in Paragraph 13[a]

Novak includes a device in which information can be stored and retrieved electronically and a plurality of electronic storage elements in a memory array. Figure 2 shows a memory device identified as block 5, which is labeled Serial Access Random Access Memory. (Brown Decl. Ex. T, Novak Fig. 2.) This memory device 5 contains a plurality of memory cells, which is shown in Figure 2 in the block labeled 10. (Brown Decl. Ex. T, Novak Fig. 2; McAlexander Decl. Ex. 2, McAlexander Report Attachment D; Invalidity Chart Based on Novak (hereinafter "Novak Chart") at D-2.) Specifically, block 10 is a memory array that includes memory sections 10a and 10b, both of which contain 32,768 memory cells. (Brown Decl. Ex. T, Novak Fig. 2; McAlexander Decl. Ex. 2, Novak Chart at D-2.)

Further, Murphy admitted that Novak describes a DRAM (Dynamic Random Access Memory). (Brown Decl. Ex. R, Murphy's Final Deposition Transcript (hereinafter "Murphy Deposition) at 601:18-21.) He also admitted that Novak describes memory cells and that Figure 2 in Novak shows two arrays of memory cells, 10-A and 10-B. (*Id*. at 601:23 - 602:1.)

2. Novak Discloses the Limitations in Paragraph 13[b]

Novak discloses receiving information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request[1] from a master, wherein the information defines the amount of one or more bits to be written to the memory array. Figure 3 shows the memory device 5 in Novak receiving block size information from a master via column addresses A6 and A7. (Brown Decl. Ex. T, Novak Fig. 3; McAlexander Decl. Ex. 2, Novak Chart at D-2.) The master is block 8 in Figure 1, which is labeled microcomputer chip. (Brown Decl. Ex. T, Novak Fig. 3; McAlexander Decl. Ex. 2, Novak Chart at D-2.) The microcomputer chip 8 includes circuitry to direct

[1] For the purposes of this motion, Hynix has used the term "request" in the manner applied by Rambus with respect to its infringement theory.

actions of the memory device 5 and thus constitutes a master. (Brown Decl. Ex. T, Novak Fig. 3; McAlexander Decl. Ex. 2, Novak Chart at D-2.) As Novak explains, "a control bus 9 coupling the microprocessor 8 to the memory 5 provides … the memory control … signals such as Address Latch, Row Address Strobe ($\overline{RAS}$), Column Address Strobe $\overline{CAS}$, Serial Select, Serial Output Enable (SOE), Write Enable, Write ($\overline{W}$), Increment (INC), etc…." (Brown Decl. Ex. T, Novak at 4:40-50; McAlexander Decl. Ex. 2, Novak Chart at D-2.)

The memory device 5 receives block size information from a master via column addresses A6 and A7 provided on input address lines 15 in Figure 2, wherein the block size information defines an amount of data. (Brown Decl. Ex. T, Novak Fig. 2; McAlexander Decl. Ex. 2, Novak Chart at D-2.) A two bit code is applied to addresses A6 and A7. (Brown Decl. Ex. T, Novak at 7:16-23; McAlexander Decl. Ex. 2, Novak Chart at D-2.) Thereafter, as Novak explains, addresses A6 and A7 "feed into the tap or register 31 as shown in FIG. 3, to determine whether one, or two, or three or all four [of the 64 bit shift] registers are accessed." (Brown Decl. Ex. T, Novak at 7:45-47; McAlexander Decl. Ex. 2, Novak Chart at D-2.) Further Novak explains that depending on the combination of the two bit code, "if the two bits are both 0, then all 256 bits in the shift register may be shifted out. If the two bits are 01, then 192 bits, starting at bit 64, may be shifted out. If the two bits are 10, then 128 bits, starting at bit 128, may be shifted out. The two bit code 11, selects the last 64 bits starting at bit number 192 and then these last 64 bits may be shifted out." (Brown Decl. Ex. T, Novak at 7:48-56; McAlexander Decl. Ex. 2, Novak Chart at D-2.) After the two bit code is applied to addresses A6 and A7, these two addresses specify the total amount of data to be transferred by selecting one of four taps along the 256 bit shift register 20 as shown in Fig 3. (Brown Decl. Ex. T, Novak at 7:42-54; McAlexander Decl. Ex. 2, Novak Chart at D-2.)

Novak also discloses one or more bits written to the memory array at a discrete point in time in response to a series of bits used to request a write of data.. The memory device 5 in Novak receives and samples a serial write request from the master, microcomputer 8, in the form of signals $\overline{TR}$ and $\overline{W}$. (McAlexander Decl. Ex. 2, Novak Chart at D-3.) These two signals, which contain bit values, must be active low when RAS goes active. (McAlexander Decl. Ex. 2, Novak Chart at D-3.). The actual write command is $\overline{W}$ active (column 6, line 51) while the state of $\overline{TR}$ determines whether the

write operation is to be a serial write or a random write (column 6, lines 35-44 and column 8, lines 30-39). (Brown Decl. Ex. T, Novak at 6:51, 6:35-44, 8:30-39; McAlexander Decl. Ex. 2, Novak Chart at D-3.) Data is sampled in response to this write request. (Brown Decl. Ex. T, Novak Fig. 4).

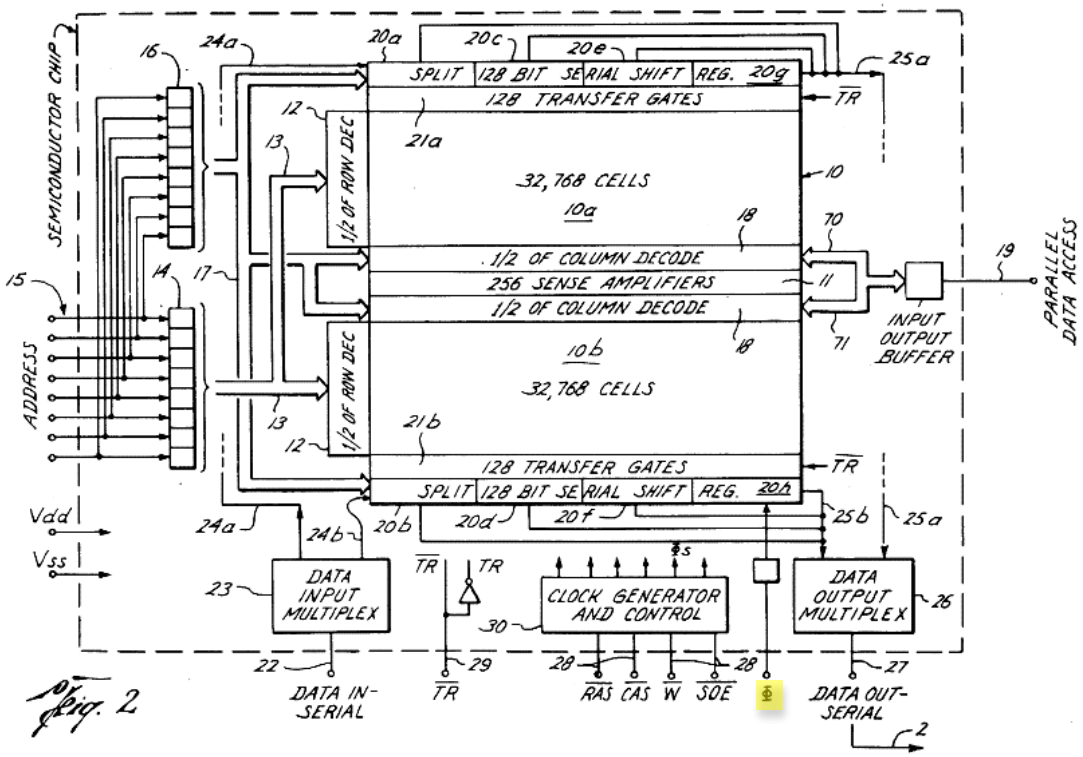
3. Novak Discloses the Limitations in Paragraph 13[c]

Novak discloses receiving a series of bits used to request a write of data to a memory device. As shown above in the immediately preceding paragraph, the memory device 5 in Novak receives a write request in the form of signals $\overline{TR}$ and $\overline{W}$ from the master 8.

4. Novak Discloses Limitation 13[d]

Novak discloses a periodic signal from a source external to the device to provide timing information, *i.e.*, an external clock signal Φ. (Brown Decl. Ex. T, Novak Figs. 2, 4.) In fact, this Court has previously held, in *Hynix I*, that in a substantially identical disclosure in Redwine, Φ constitutes an external clock signal. (Brown Decl. Ex. S, Redwine MSJ Order at 5; *see also* McAlexander Decl. ¶ 3.) By comparing the external clock signal Φ of Redwine (Fig. 2-f) and Novak (Fig. 4-f), as well as the block diagrams of the memory devices in Redwine (Fig. 1) and Novak (Fig. 2), it is apparent that Novak discloses the same external clock signal Φ:

NOVAK



REDWINE

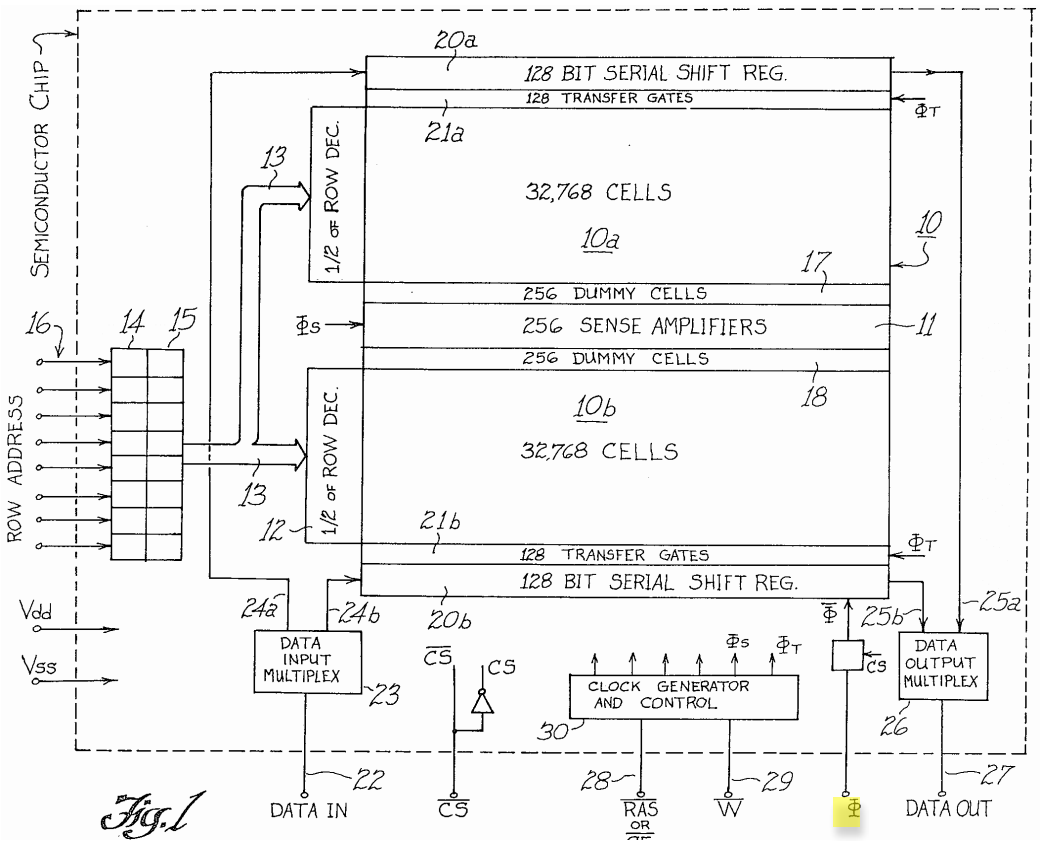


Fig. 1

(Brown Decl. Ex. V, Redwine Figs. 1, 2; Brown Decl. Ex. T, Novak Figs. 2, 4; *see also* McAlexander Decl. ¶ 3 ("[T]he Φ and $\overline{W}$ signals disclosed in Redwine are identical to the Φ and $\overline{W}$ signals disclosed in Novak.")). As such, this Court should conclude, consistent with its prior holding, that Novak discloses an external clock signal. (Brown Decl. Ex. S, Redwine MSJ Order at p. 4.)

Novak further discloses obtaining at a discrete point in time a first portion of one or more bits written to a memory array and a second portion of said one or more bits written to a memory array with said discrete point in time having a known timing relationship to a first transition of an external clock signal. As shown by waveforms e and f in Figure 4, first and second portions (*i.e.*, data bits) of the first amount of data are sampled by memory device 5 in response to the write request (which includes the bit values of $\overline{W}$ and $\overline{TR}$ signals) synchronously with respect to first and second transitions of the external clock signal Φ. (Brown Decl. Ex. T, Novak at 10:18-37, 7:48-56, 8:36-39; McAlexander Decl. Ex. 2, Novak Chart at D-3.) As indicated at Figure 4e and 4f, the write data is obtained at discrete points of time defined by the transitions of the external clock signal Φ.

In addition, the write request signals $\overline{W}$ and $\overline{TR}$ have a known timing relationship (as interpreted by Rambus) to the external clock signal Φ, as Φ governs the timing of the generation of control signals such as $\overline{W}$ and $\overline{TR}$. (McAlexander Decl. Ex. 2, Novak Chart at D-16.) Moreover, one skilled in this art would know the $\overline{W}$, $\overline{TR}$ and Φ signals are generated in relation to a system clock, and therefore have a known timing relationship (as interpreted by Rambus) with one another. (*Id.* at D-2.) *See Helifix,* 208 F.3d 1339 (element need not be disclosed in words for reference to anticipate if one skilled in the art would understand the publication to disclosed the element). Further, Finally, even Rambus's own expert, Mr. Murphy, admitted that data is input and output synchronously with respect to the external clock signal Φ. (Brown Decl. Ex. R, Murphy Deposition at 605:23 - 606:19.)

5. Novak Anticipates Asserted Claim 14

Novak discloses sampling a first portion of data at a time with a known timing relationship (as interpreted by Rambus) to a rising edge transition of the external clock signal and sampling a second portion of data at a time with a known timing relationship (as interpreted by Rambus) to a falling edge transition of the external clock signal. In Novak, waveforms e and f in Figure 4 show dual edge clocking in that 256 bits of data is input in 128 clock cycles. (Brown Decl. Ex. T, Novak Fig. 4; McAlexander Decl. Ex. 2, Novak Chart at D-4**.)** These waveforms indicate that a first portion of the data (e.g., one half of the 256 bits) is sampled with a known timing relationship to a rising edge transition of the external clock signal Φ and a second portion of the data (*e.g.*, the other half of the 256 bits of data) is sampled with a known timing relationship to falling edge transition of the external clock signal Φ. (Brown Decl. Ex. T, Novak at 6:32-36, 6:63-68; McAlexander Decl. Ex. 2, Novak Chart at D-4.) As Novak explains, the "shift clock signal Φ … may move 256 bits … at two stages or bits per clock cycle, requiring 128 clock cycles …." . (Brown Decl. Ex. T, Novak at 6:32-36, 6:63-68; McAlexander Decl. Ex. 2, Novak Chart at D-4.) Thus, data is sampled a known timing relationship to both rising and falling edge transitions of the external clock signal.

Further, Mr. Murphy admitted that, in Novak, one bit of data is input on the high pulse in Figure 4d while another bit is input on the low pulse. (Brown Decl. Ex. R, Murphy Deposition at 604:19-22.) Additionally, Mr. Murphy admitted that for read transactions (Fig. 4-d) of Novak, which

operate similarly to write transactions, "one piece of data out for each positive pulse and one piece out for each negative pulse." (*Id*. at 609:21-610:1). Therefore, Mr. Murphy admits that the data in Novak is sampled with respect to a rising (high or positive) transition and a falling (low or negative) transition of the external clock signal Φ.

Because each and every element of Claim 14 of the '184 patent (including the elements of the claim from which it depends) is disclosed by Novak, this claim is anticipated and invalid under 35 U.S.C. § 102.

B. NOVAK ANTICIPATES ASSERTED CLAIM 43 OF THE '051 PATENT

Independent claim 34 and dependent, asserted claim 43 of the '051 patent are invalid under 35 U.S.C. § 102 because each and every limitation of those claims is disclosed by the Novak patent. The following table provides the language of claims 34 and 43 of the '051 patent and the corresponding claim constructions:

'051 Claim Language	Claim Constructions
34[a]. A memory device having a plurality of memory arrays, the memory device comprising:	"memory device" means "a device in which information can be stored and retrieved electronically"
[b] first input receiver circuitry to receive an operation code synchronously with respect to an external clock; and	"input receiver circuitry" means "circuitry on the device to receive one or more signals from an external source" "operation code" means "one or more bits to specify a type of action" "synchronously with respect to" means "having a known timing relationship with respect to" "external clock signal" means "a periodic signal from a source external to the device to provide timing information"
[c] second input receiver circuitry to sample data, in response to the operation code, after a predetermined number of clock cycles of the external clock.	"sample" means "to obtain at a discrete point in time" "data" means "one or more bits written to/read from a memory array"
43. The memory device of claim 34 wherein the memory device is a synchronous dynamic random access memory.	"synchronous dynamic random access memory" means "a synchronous semiconductor memory device which includes one or more arrays of DRAM cells" "synchronous memory device" means "a memory device that receives an external clock signal which governs the timing of the response to a transaction request."

1. Novak Discloses the Limitations in Paragraph 34[a]

Novak discloses a plurality of devices in which information can be stored and retrieved electronically. As shown above with respect to the preamble of claim 13 of the '184 patent, Novak discloses a memory device 5, which includes memory 10, which includes memory arrays 10a and 10b, both of which contain 32,768 memory cells.

2. Novak Discloses the Limitations in Paragraph 34[b]

Novak discloses circuitry on the device to receive one or more signals from an external source, said signals including one or more bits to specify a type of action. This Court has previously held that signal $\overline{W}$ in Redwine constituted an operation code. (Brown Decl. Ex. S, Redwine MSJ Order at p. 5.) Again, by comparing the $\overline{W}$ signal of Redwine (Fig 4-b) with the $\overline{W}$ signal of Novak (Fig. 4-b) as well as the block diagram of the memory device in Redwine (Fig. 1) with that in Novak (Fig. 2), it is apparent that Novak discloses the same signal $\overline{W}$:

NOVAK

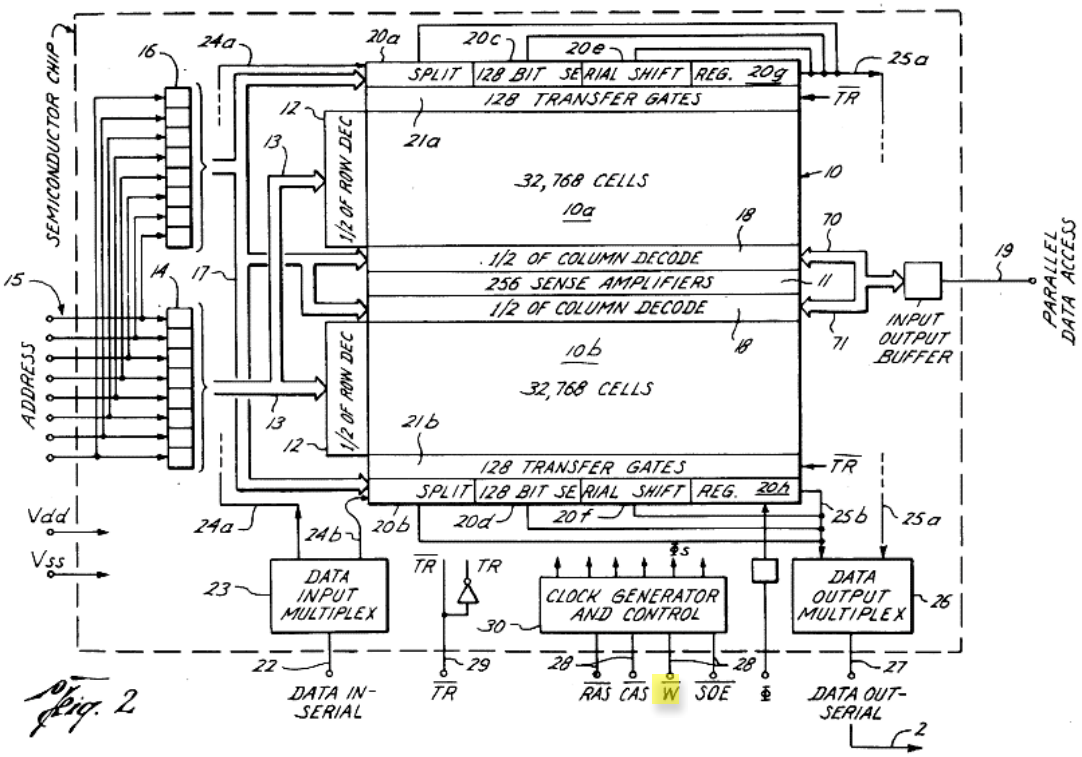


Fig. 2

REDWINE

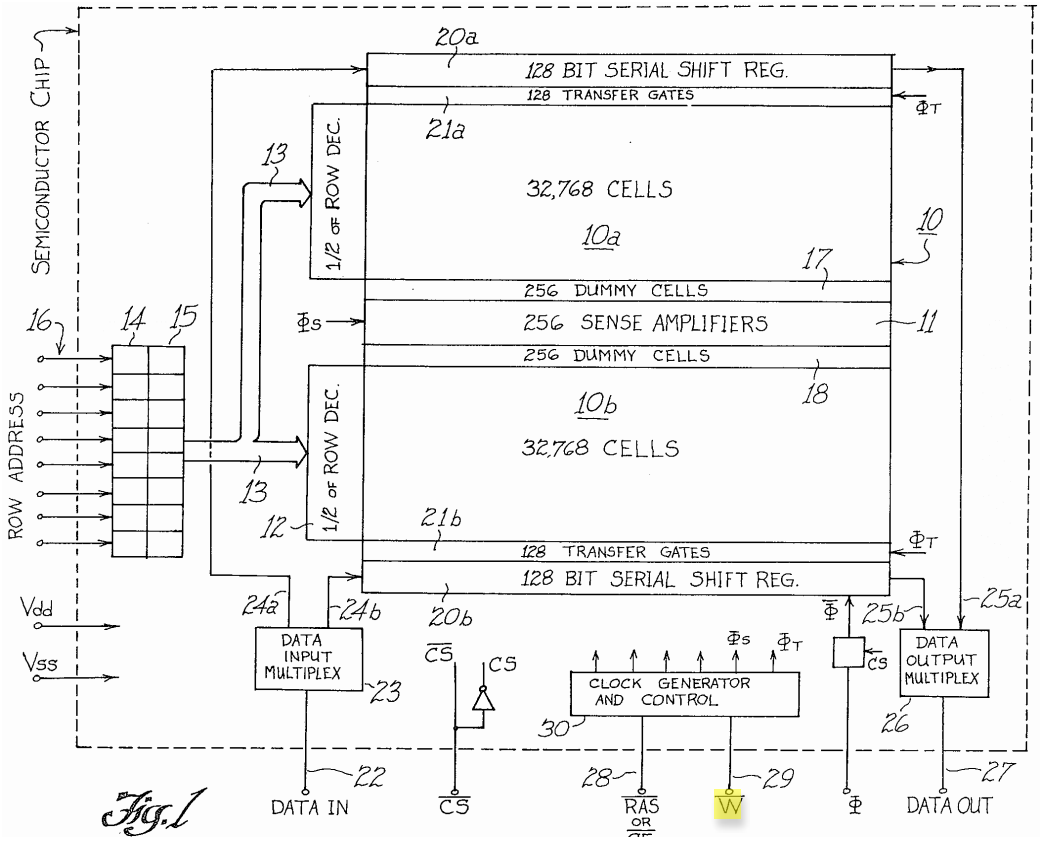


Fig. 1

(Brown Decl. Ex. V, Redwine Figs. 1, 2; Brown Decl. Ex. T, Novak Figs. 2, 4; McAlexander Decl. ¶ 3 ("[T]he Φ and $\overline{W}$ signals disclosed in Redwine are identical to the Φ and $\overline{W}$ signals disclosed in Novak.") As such, this Court should conclude that Novak, like Redwine, discloses an operation code in the form of the signal $\overline{W}$.

Additionally, Novak discloses an operation code in the form of the signals $\overline{W}$ and $\overline{TR}$. (*See* McAlexander Decl. Ex. 2, Novak Chart at D-51.) Signals $\overline{W}$ and $\overline{TR}$ specify a type of action (*e.g.*, serial read or serial write operation) as shown in the Figure 4 timing diagram. (*See also* Brown Decl. Ex. T, Novak at 8:32-37 ("For a serial read operation, $\overline{TR}$ goes to active-low and the $\overline{W}$ signal is held high during the period seen in FIG. 4b. … For a serial write operation, the $\overline{TR}$ and $\overline{W}$ signal must both be active-low as also seen in FIG. 4b.)). Thus, the values of $\overline{W}$ and $\overline{TR}$ signals constitute an operation code; when both of these signals are low when RAS goes active, these signals specify a serial write operation. (McAlexander Decl. Ex. 2, Novak Chart at D-51.) When $\overline{W}$ is low and $\overline{TR}$ is high, these signals specify a random write operation. (McAlexander Decl. Ex. 2, Novak Chart at D-51.)

In Novak, the input receiver circuitry in memory device 5 receives the operation code $\overline{W}$ and $\overline{TR}$ at a time that has a known timing relationship (as interpreted by Rambus) to an external clock signal. (McAlexander Decl. Ex. 2, Novak Chart at D-14-15.) Figure 2 of Novak shows that when the memory device is accessed, it samples the $\overline{W}$ and $\overline{TR}$ signals, which as described above, constitute an operation code. (McAlexander Decl. Ex. 2, Novak Chart at D-14-15.) As demonstrated above in connection with the limitations in 13[d] of the '184 patent, the $\overline{W}$ and $\overline{TR}$ signals have a known timing relationship (as interpreted by Rambus) to the external clock signal Φ.

3. Novak Discloses the Limitations in Paragraph 34[c]

Novak discloses second input receiver circuitry to sample data, in response to the operation code, after a predetermined number of clock cycles of the external clock. In Novak, block 23 labeled data input multiplex in Figure 2 discloses a second input receiver circuitry. (Brown Decl. Ex. T, Novak at 6:24-28; McAlexander Decl. Ex. 2, Novak Chart at D-15.) This receiver samples an operation code after a predetermined number of clock cycles. Novak discloses that data can be read and written into a desired portion of the shift register 20 of the DRAM at the same time, as shown in Figs. 4d and 4e. (Brown Decl. Ex. T, Novak at 13:52-55, Fig. 4; McAlexander Decl. Ex. 2, Novak Chart at D-15.) It would be known to one of ordinary skill in the art, and as shown in Figs. 4d and 4e, that the start of writing data is delayed by at least one half clock cycle (a "predetermined number") from the start of reading data in order to accomplish reading and writing into shift register 20 during the same period. (McAlexander Decl. Ex. 2, Novak Chart at D-15.)

4. Novak Anticipates Asserted Claim 43 of the '051 Patent

Novak discloses a memory device that receives an external clock signal which governs the timing of the response to a transaction request (*e.g.*, the timing of outputting of data in a serial read or serial write operation). (*See, e.g.*, Brown Decl. Ex. T, Novak Fig. 6, 13:6-20; McAlexander Decl. Ex. 2, Novak Chart at D-15-16.) Novak further discloses a "dynamic" memory device; the memory cells are of a "one-transistor type" (Brown Decl. Ex. T, Novak at 5:5-6), which would be understood by one of ordinary skill in the art to refer to dynamic random access memory cells. (Brown Decl. Ex. T, Novak at 5:5-6; McAlexander Decl. Ex. 2, Novak Chart at D-15-16.)

Because each and every element of Claim 43 of the '051 patent (including the elements of the

claim from which it depends) is disclosed by Novak, this claim is anticipated and invalid under 35 U.S.C. § 102.

C. NOVAK ANTICIPATES ASSERTED CLAIM 16 OF THE '863 PATENT

Independent claim 14 and dependent claims 15 and 16 of the '863 patent are invalid under 35 U.S.C. § 102 because each and every limitation of those claims is disclosed by the Novak patent. The following table provides the language of claims 14, 15, and 16 of the '863 patent and the corresponding claim constructions:

'863 Claim Language	Claim Constructions
14[a]. A method of operation in a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:	"synchronous memory device" mean "a device that receives an external clock signal which governs the timing of the response to a transaction request" "memory device" means "a device in which information can be stored and retrieved electronically"
[b] receiving first block size information from a memory controller, wherein the memory device is capable of processing the first block size information, wherein the first block size information represents a first amount of data to be input by the memory device in response to an operation code;	"block size information" means "information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request" "data" means "one or more bits written to/read from a memory array" "operation code" means "one or more bits to specify a type of action"
[c] receiving the operation code, from the memory controller, synchronously with respect to an external clock signal; and	"synchronously with respect to" means "having a known timing relationship with respect to" "external clock signal" means "a periodic signal from a source external to the device to provide timing information"
[d] inputting the first amount of data in response to the operation code.	"synchronous memory device" mean "a device that receives an external clock signal which governs the timing of the response to a transaction request" "memory device" means "a device in which information can be stored and retrieved electronically"
15. The method of claim 14 wherein inputting the first amount of data includes receiving the first amount of data synchronously with respect to the external clock signal.	
16. The method of claim 15 wherein the first amount of data is sampled over a plurality of clock cycles of the external clock signal.	

1. Novak Discloses the Limitations in Paragraph 14[a]

As shown above in the preamble of claim 14 of the '863 patent and claim 43 of the '051 patent, Novak discloses a synchronous dynamic random access memory device having at least one memory section including a plurality of memory cells.

2. Novak Discloses the Limitations in Paragraph 14[b]

As shown above in connection with the limitations in 13[b] of the '184 patent, Novak discloses a memory device which processes block size information from a memory controller in response to an operation code. The microcomputer chip 8 is a memory controller, *i.e.*, it controls the operation of the memory device.

Further, as shown above in connection with the limitations in 13[b] of the '184 patent, the memory device 5 is capable of receiving or processing block size information. Novak discloses that "the tap address bits may be used for shifting data into the selected portion of the shift register." (Brown Decl. Ex. T, Novak at 7:54-56; McAlexander Decl. Ex. 2, Novak Chart at D-33.) Additionally, as shown above in connection with the limitations in 13[b] of the '184 patent, Novak discloses block size information which defines an amount of data to be input.

3. Novak Discloses the Limitations in Paragraph 14[c]

Novak discloses receiving an operation code in a known timing relationship to the external clock signal. As shown above in the limitations in 34[b] of the '051 patent, the Novak memory device receives operation code in a known timing relationship with respect to an external clock signal. As shown above in the limitations in 14[b] of the '863 patent, data is input in response to the operation code**.**

4. Novak Anticipates Claim 15

Novak discloses inputting data synchronously (*i.e.*, in a known timing relationship) with an external clock signal. As shown above in connection with the limitations in 13[d] of the '184 patent, data is received synchronously (*i.e.*, in a known timing relationship) with respect to the external clock signal Φ.

5. Novak Anticipates Asserted Claim 16

Novak discloses obtaining one or more bits written to a memory array at a discrete point in time over a plurality of clock cycles of the external clock signal. As shown in the Novak timing diagram (Figure 4), the total amount of data defined by addresses A6 and A7 (*i.e.*, waveform h) is sampled over a plurality of clock signals of external clock Φ. (Brown Decl. Ex. T, Novak at 10:28-36 ("The two bit tap address, see FIG. 4h, appearing on the most significant column address lines when CAS goes low, see FIG. 4g, determines which of the four cascaded 64-bit shift registers will be connected to serial output 27. The serial shift clock Φ, FIG 4f, then shifts the data out of the shift register at the desired data rate in response to the frequency of the clock Φ.")). (McAlexander Decl. Ex. 2, Novak Chart at D-35.) Novak further provides for writing data to the shift register in a similar fashion. (Brown Decl. Ex. T, Novak at 7:53-55; McAlexander Decl. Ex. 2, Novak Chart at D-35.)

Because each and every element of Claim 16 of the '863 patent (including the elements of the claims from which it depends) is disclosed by Novak, this claim is anticipated and invalid under 35 U.S.C. § 102.

D. NOVAK ANTICIPATES ASSERTED CLAIM 33 OF THE '120 PATENT

Independent claim 26 and dependent claims 29 and 33 of the '120 patent are invalid under 35 U.S.C. § 102 because each and every limitation of those claims is disclosed by the Novak patent. The following table provides the language of claims 14, 15, and 16 of the '863 patent and the corresponding claim constructions:

'120 Claim Language	Claim Constructions
26[a]. A synchronous dynamic random access memory device having at least one memory section including a plurality of memory cells, the memory device comprising:	"synchronous memory device" means "a memory device that receives an external clock signal which governs the timing of the response to a transaction request"
[b] clock receiver circuitry to receive an external clock signal;	"external clock signal" means "a periodic signal from a source external to the device to provide timing information"

'120 Claim Language	Claim Constructions
[c] input receiver circuitry, including a first plurality of input receivers to sample block size information synchronously with respect to the external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a first operation code; and	"sample" means "to obtain at a discrete point in time" "block size information" means "information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request" "synchronously with respect to" means "having a known timing relationship with respect to" "operation code" means "one or more bits to specify a type of action"
[d] a plurality of output drivers to output the amount of data in response to the first operation code.	
29. The memory device of claim 26 wherein the input receiver circuitry samples the first operation code synchronously with respect to the external clock signal.	
33. The memory device of claim 29 wherein the first operation code includes precharge information.	"precharge information" means "one or more bits indicating whether the sense amplifiers and/or bits lines (or a portion of the sense amplifiers and/or bits lines) should be precharged"

1. Novak Discloses the Limitations in Paragraph 26[a]

As shown above with respect to the preamble of claim 14 of the '863 patent, Novak discloses a synchronous dynamic random access memory device having at least one memory section including a plurality of memory cells.

2. Novak Discloses the Limitations in Paragraph 26[b]

Novak discloses a circuit for adjusting the timing relationship between a clock signal and another signal. In Novak, Figure 6 shows a memory device 5 including 8 memory chips. (Brown Decl. Ex. T, Novak Fig. 6; McAlexander Decl. Ex. 2, Novak Chart at D-18.) Each of the DRAM chips within the memory device 5 receives an external clock signal Φ. (McAlexander Decl. Ex. 2, Novak Chart at D-18.)

Novak further discloses a periodic signal (Φ) from a source external to the device to provide timing information, as demonstrated above under the limitations in 13[d] of the '184 patent.

3. Novak Discloses the Limitations in Paragraph 26[c]

Novak discloses input receiver circuitry including a first plurality of input receivers to sample block size information synchronously (*i.e.*, in a known timing relationship) with respect to an external

clock signal. In Novak, Figure 2 shows an input receiver 16, which samples block size information via address inputs 15. (Brown Decl. Ex. T, Novak Fig. 2.; McAlexander Decl. Ex. 2, Novak Chart at D-18-19.) Input receiver 16 further contains a plurality of input receivers in that it contains a plurality of address latches. (Brown Decl. Ex. T, Novak Fig. 2.; McAlexander Decl. Ex. 2, Novak Chart at D-18-19.) Two of the column address latches 16 receive the block size information via column address A6 and A7. (Brown Decl. Ex. T, Novak Fig. 2.; McAlexander Decl. Ex. 2, Novak Chart at D-18-19.) As Novak explains, "[a] column address is also received on the input pins 15 and latched into column address latches 16." (Brown Decl. Ex. T, Novak at 5:56-57; McAlexander Decl. Ex. 2, Novak Chart at D-18-19.)

This input receiver circuitry receives an operation code synchronously with respect to an external clock signal. The address latches in input receiver circuitry receive block size information synchronously with respect to the $\overline{\text{RAS}}$ signal because there is a known timing relationship (as interpreted by Rambus) between the time when address latches receive and latch the block size information and when $\overline{\text{RAS}}$ goes low. (McAlexander Decl. Ex. 2, Novak Chart at D-18-19.) As Novak explains, "when $\overline{\text{RAS}}$ goes low as seen in Fig 4a, clocks derived from $\overline{\text{RAS}}$ cause the buffers 14 to accept and latch the eight row address bits then appearing on the input lines 15." (Brown Decl. Ex. T, Novak at 8:25-28.) There is also a known timing relationship (as interpreted by Rambus) between $\overline{\text{RAS}}$ and the external clock signal Φ. (McAlexander Decl. Ex. 2, Novak Chart at D-18-19.) Further, one skilled in this art would know that $\overline{\text{RAS}}$ and Φ are generated in relation to a system clock, and have a known timing relationship (as interpreted by Rambus) with one another; such knowledge by one of skill in the art is sufficient to establish anticipation. (McAlexander Decl. Ex. 2, Novak Chart at D-18-19.) *In re Graves,* 69 F.3d at 1152. Even Mr. Murphy admitted that RAS was generated with particular timing references with respect to the system clock. (Brown Decl. Ex. R, Murphy Deposition at 725:1-10.) Thus, because the address latches receive block size information synchronously with respect to $\overline{\text{RAS}}$, and because the $\overline{\text{RAS}}$ signal has a known timing relationship (as interpreted by Rambus) with external clock signal Φ, it follows that the address latches receive block size information synchronously with respect to external clock signal Φ. (McAlexander Decl. Ex. 2, Novak Chart at D-18-19.)

As shown above in connection with the limitations in 13[c] of the '184 patent, Novak further discloses block size information that defines an amount to output by the memory device 5 in response to a first operation code.

4. Novak Discloses the Limitations in Paragraph 26[d]

Novak discloses a plurality of output drivers. In Novak, output drivers are included in Block 26 in Figure 2. (Brown Decl. Ex. T, Novak Fig. 2; McAlexander Decl. Ex. 2, Novak Chart at D-19-20.) These output drivers output data in response to a operation code. As mentioned above in connection with the limitations in 34[b] of the '051 patent and pursuant to the *Hynix* I case, Novak discloses an operation code.

5. Novak Anticipates Claim 29

As shown above in connection with the limitations in 34[b] of the '051 patent, the memory device 5 in Novak has input receiver circuitry that receives or samples the first operation code in a known timing relationship (as interpreted by Rambus) with respect to the external clock signal.

6. Novak Anticipates Asserted Claim 33

Novak discloses "one or more bits indicating whether the sense amplifiers and/or bits lines (or a portion of the sense amplifiers and/or bits lines) should be precharged." In Novak, the operation code not only includes the bit values of $\overline{W}$ and $\overline{TR}$ signals but also includes the bit value of $\overline{RAS}$ signal. (McAlexander Decl. Ex. 2, Novak Chart at D-21.) The $\overline{RAS}$ signal in Novak represents a bit value in the operation code that indicates whether the sense amplifiers and/or bits lines should be precharged. (McAlexander Decl. Ex. 2, Novak Chart at D-21.) The sense amplifiers in Novak are labeled "256 sense amplifiers" and are represented by block 11 in Figure 2. (Brown Decl. Ex. T, Novak Fig. 2; McAlexander Decl. Ex. 2, Novak Chart at D-21.)

Specifically, as was known in the art when $\overline{RAS}$ goes high, the precharge portion of the read or write cycle is activated. Indeed, Novak specifically references the operation of the memory device described in U.S. Pat. No. 4,239,993, (Brown Decl. Ex. T, Novak at 5:3-8), which expressly describes the use of $\overline{RAS}$ to start a precharge operation, (Brown Decl. Ex. U, U.S. Pat. No. 4,239,993 (hereinafter "McAlexander Patent") at 5:60-62). (*See also*, McAlexander Decl. Ex. 2, Novak Chart at D-21.) Precharging is a necessary operation to prepare the sense amplifiers for subsequent memory

operations. As explained in U.S. Pat. No. 4,239,993, the precharge step occurs in response to a $\overline{RAS}$ transition after the completion of the active portion of the read or write cycle. (Brown Decl. Ex. U, McAlexander Patent at 5:60:62.) Precharge information within the operation code is, therefore, the bit value of the $\overline{RAS}$ signal.

Additionally, precharge information is disclosed in Novak in the form of a refresh operation. As explained in Novak, "when a row is addressed for serial-read or serial write, this also refreshes the data in this row." (Brown Decl. Ex. T, Novak at 14:4-7; McAlexander Decl. Ex. 2, Novak Chart at D-21.) Further, even Mr. Murphy testified that a refresh operation requires precharging. (Brown Decl. Ex. R, Murphy Deposition at 749:6-22.) Therefore, one of ordinary skill in the art would understand that a command initiation the serial-read or serial-write operation necessarily includes a refresh operation which contains one or more bits indicating whether the sense amplifiers and/or bits lines (or a portion of the sense amplifiers and/or bits lines) should be precharged. (McAlexander Decl. Ex. 2, Novak Chart at D-21.)

Because each and every element of claim 33 of the '120 patent (including the elements of the claims from which it depends) is disclosed by Novak, this claim is anticipated and invalid under 35 U.S.C. § 102.

E. NOVAK ANTICIPATES ASSERTED CLAIM 3 OF THE '446 PATENT

Independent claim 1 and dependent claims 2 and 3 of the '446 patent are invalid under 35 U.S.C. § 102 because each and every limitation of those claims is disclosed by the Novak patent. The following table provides the language of claims 1, 2, and 3 of the '446 patent and the corresponding claim constructions:

'446 Claim Language	Claim Constructions
1[a]. A synchronous integrated circuit device having a memory array which includes dynamic random access memory cells, wherein the integrated circuit device comprises:	"integrated circuit device" means "a circuit constructed on a single monolithic substrate, commonly called a 'chip.'"
[b] a clock receiver to receive an external clock signal	"clock receiver circuitry" means "a circuit for adjusting the timing relationship between a clock signal and another signal" "external clock signal" means "a periodic signal from a source external to the device to provide timing information"

'446 Claim Language	Claim Constructions
[c] a plurality of sense amplifiers, coupled to the memory array, to sense data from the dynamic random access memory cells; and	"sample" means "to obtain at a discrete point in time" "block size information" means "information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request" "synchronously with respect to" means "having a known timing relationship with respect to" "operation code" means "one or more bits to specify a type of action"
[d] a plurality of input receivers to sample an operation code synchronously with respect to the external clock signal, the operation code including precharge information, wherein, in response to the precharge information, the plurality of sense amplifiers is automatically precharged after the data is sensed.	"sample" means "to obtain at a discrete point in time" "precharge information" means "one or more bits indicating whether the sense amplifiers and/or bits lines (or a portion of the sense amplifiers and/or bits lines) should be precharged"
2. The integrated circuit device of claim 1 wherein the operation code specifies a read operation, and wherein the integrated circuit device further includes a plurality of output drivers to output first and second portions of the data in response to the operation code specifying a read operation.	
3. The integrated circuit device of claim 2 wherein the plurality of output drivers output the first portion of the data synchronously with respect to a rising edge transition of the external clock signal; and the plurality of output drivers output a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.	

1. Novak Discloses the Limitations in Paragraph 1[a]

In Novak, Figure 2 shows a circuit constructed on a single monolithic substrate, commonly called a "chip." As explained in Novak, "[the memory device 5 depicted in Fig. 2 is typically made by an N-channel, MOS process, with all of the device being included in one silicon chip." (Brown Decl. Ex. T, Novak at 5:20-23; McAlexander Decl. Ex. 2, Novak Chart at D-37.) Further, he memory device 5 is labeled as "SEMICONDUCTOR CHIP." (Brown Decl. Ex. T, Novak Fig. 2; McAlexander Decl. Ex. 2, Novak Chart at D-37.)

2. Novak Discloses the Limitations in Paragraph 1[b]

As shown above in connection with the limitations in 26[b] of the '120 patent, Novak discloses a clock receiver to receive an external clock signal.

3. Novak Discloses the Limitations in Paragraph 1[c]

As shown above in connection with the limitations in claim 33 of the '120 patent, the sense amplifiers in Novak are labeled "256 sense amplifiers" and are represented by block 11 in Figure 2. (Brown Decl. Ex. T, Novak Fig. 2.)

4. Novak Discloses the Limitations in Paragraph 1[d]

Novak discloses a plurality of input receivers to sample an operation code synchronously with respect to the external clock signal, the operation code including precharge information, wherein, in response to the precharge information, the plurality of sense amplifiers is automatically precharged after the data is sensed.

As shown above in connection with the limitations in paragraph 34[b] of the '051 patent, in Novak, the memory device 5 has input receiver circuitry which receives or samples the first operation code in a known timing relationship (as interpreted by Rambus) with respect to the external clock signal.

As shown above in connection with the limitations in claim 33 of the '120 patent, in Novak, the operation code includes precharge information. This claim specifically requires that plurality of sense amplifiers is automatically precharged after the data is sensed in response to the precharge information. As Novak explains and mentioned above, "when a row is addressed for serial-read or serial write, this also refreshes the data in this row." (Brown Decl. Ex. T, Novak at 14:4-7; McAlexander Decl. Ex. 2, Novak Chart at D-38-39.)

5. Novak Anticipates Claim 2

Novak discloses a plurality of output drivers to output first and second portions of the data in response to the operation code specifying a read operation. As mentioned above pursuant to the *Hynix I* case, Novak discloses an operation code (which includes the bit values of the $\overline{W}$ and $\overline{TR}$ signals). In Figure 3, an output driver coupled to the output of decoder block 31 is shown driving output terminal 27. (McAlexander Decl. Ex. 2, Novak Chart at D-39-40.) The output driver in Figures 2 and 3 outputs data in response to the operation code as shown in the Figure 4 timing diagram. (Brown Decl. Ex. T, Novak at 10:18-34; McAlexander Decl. Ex. 2, Novak Chart at D-39-40.) In Figure 6, each of the eight memory chips includes an output driver. Thus, in the embodiment wherein the eight memory

chips in Figure 6 are integrated in a single chip, the resulting chip has a plurality of output drivers. (Brown Decl. Ex. T, Novak at 12:60-62; McAlexander Decl. Ex. 2, Novak Chart at D-39-40.)

6. Novak Anticipates Asserted Claim 3

As demonstrated above connection with in the limitations in claims 13 and 14 of the '184 patent, Novak discloses reading a first portion of data out in a known timing relation (as interpreted by Rambus) with respect to a rising edge transition of the external clock signal and reading out a second portion of data in a known timing relation with respect to a falling edge transition of the external clock signal.

Because each and every element of claim 3 of the '446 patent (including the elements of the claims from which it depends) is disclosed by Novak, this claim is anticipated and invalid under 35 U.S.C. § 102.

F. NOVAK ANTICIPATES CLAIM 34 OF THE '037 PATENT

Independent claim 34 of the '037 patent is invalid under 35 U.S.C. § 102 because each and every limitation of those claims is disclosed by the Novak patent. The following table provides the language of claim 34 of the '037 patent and the corresponding claim constructions:

'037 Claim Language	Claim Constructions
34[a]. A method of operation of a synchronous dynamic random access memory device, wherein the method comprises:	"synchronous memory device" means "a memory device that receives an external clock signal which governs the timing of the response to a transaction request"
[b] sampling an operation code synchronously with respect to an external clock signal, wherein the operation code specifies that the memory device sample data to be written into a plurality of dynamic memory cells, and wherein the operation code further specifies that the memory device precharge a plurality of sense amplifiers	"sample" means "to obtain at a discrete point in time" "synchronously with respect to" means "having a known timing relationship with respect to" "external clock signal" means "a periodic signal from a source external to the device to provide timing information" "operation code" means "one or more bits to specify a type of action"
[c] sampling the data, in response to the operation code, after a delay time transpires	
[d] sampling address information to identify a subset of the plurality of dynamic memory cells	
[e] writing the data to the subset of the plurality of dynamic memory cells using the plurality of sense amplifiers; and	

'037 Claim Language	Claim Constructions
[f] precharging the plurality of sense amplifiers in response to the operation code, wherein the plurality of sense amplifiers is precharged automatically after the data is written.	

1. Novak Discloses the Limitations in Paragraph 34[a]

As shown above in connection with the limitations in the preamble of claim 14 of the '863 patent, Novak discloses a synchronous dynamic random access memory device.

2. Novak Discloses the Limitations in Paragraph 34[b]

Novak discloses sampling an operation code synchronously with respect to an external clock signal, wherein the operation code specifies that the memory device sample data to be written into a plurality of dynamic memory cells, and wherein the operation code further specifies that the memory device precharge a plurality of sense amplifiers. As shown above in connection with the limitations in 13[b] of the '184 patent, $\overline{W}$ and $\overline{TR}$ are operation codes that specify that the memory device sample data to be written. As shown above in connection with the limitations in 34[b] of the '051 patent, the memory device 5 samples operation code synchronously with respect to the external clock signal. As shown above in connection with the limitations in claim 33 of the '120 patent, the operation code includes precharge information. As shown above in connection with the limitations of 1[d] of the '446 patent, Novak discloses precharging the plurality of sense amplifiers in response to the operation code.

3. Novak Discloses the Limitations in Paragraph 34[c]

Novak discloses sampling the data, in response to the operation code, after a delay time transpires. As described above in connection with the limitations in 34[c] of the '051 patent, Novak describes the memory device 5 sampling data in response to the operation code after a predetermined number of clock cycles of the external clock signal Φ. Sampling data after a predetermined number of clock cycles of the external clock signal Φ constitutes a delay time.

4. Novak Discloses the Limitations in Paragraph 34[d]

Novak discloses sampling address information to identify a subset of the plurality of dynamic memory cells. As shown in limitation 26[c] of the '120 patent, memory device 5 samples address information via address inputs 15. (Brown Decl. Ex. T, Novak Fig. 2; McAlexander Decl. Ex. 2,

Novak Chart at D-53.) The memory device includes address latches 16, which receive address information. (McAlexander Decl. Ex. 2, Novak Chart at D-53.) One of ordinary skill in the art would understand that "latching" information is the same as "sampling" information, since a latch operates to capture information at discrete points. (McAlexander Decl. Ex. 2, Novak Chart at D-53.)

5. Novak Discloses the Limitations in Paragraph 34[e]

Novak discloses writing the data to the subset of the plurality of dynamic memory cells using the plurality of sense amplifiers. In Novak, as part of the write operation, the input data is driven into the corresponding sense amplifiers, which then write the data to the array. (Brown Decl. Ex. T, Novak at 6:50-54; McAlexander Decl. Ex. 2, Novak Chart at D-33.)

6. Novak Discloses the Limitations in Paragraph 34[f]

As shown above in connection with the limitations in 1[d] of the '446 patent, Novak discloses precharging the plurality of sense amplifiers in response to the operation code, wherein the plurality of sense amplifiers is precharged automatically after the data is written.

Because each and every element of claim 34 of the ‘037 patent (including the elements of the claims from which it depends) is disclosed by Novak, this claim is anticipated and invalid under 35 U.S.C. § 102.

VI. CONCLUSION

For the reasons stated and under the authorities cited, Hynix, Micron, and Samsung respectfully request that the Court grant its motion for summary judgment that the claims at issue of U.S. Patent Nos. 6,182,184, 6,324,120, 6,452,863, 6,546,446, 6,314,051, and 6,584,037 are invalid as anticipated by Novak.

DATED: October 24, 2008 Respectfully submitted,

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